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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,238	11/12/2003	Makiko Kan	09792909-5719	6389

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EXAMINER

LIN, SUN J

ART UNIT PAPER NUMBER

2825

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/706,238	Applicant(s) KAN, MAKIKO	
	Examiner Sun J. Lin	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 12 November 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 2, 9 and 10 is/are rejected.
- 7) ☒ Claim(s) 3-8 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

1. This office action is in response to application 10/706,238 filed on 11/12/2003.  
Claims 1 – 10 remain pending in the application.

#### *Specification Objections*

- 2 The specification is objected to because of following informalities:  
Page 8, line 3, change "circuit 1" to **—circuit 101—**.

Appropriate correction is required.

#### *Claim Objections*

3. Claims listed below are objected to because of the following informalities:

Claim 1, line 8, before "first" insert **—different—**.  
Claim 1, line 11, before "first" insert **—different—**.  
Claim 1, line 16, before "first" insert **—different—**.  
Claim 2, line 1, change "A" to **—The—**.  
Claim 2, line 3, before "first" insert **—plurality of different—**.  
Claim 2, line 5, before "second" insert **—identified—**.  
Claim 3, line 1, change "A" to **—The—**.  
Claim 3, line 2, before "first" insert **—different—**.  
Claim 3, line 7, before "combining" insert **—by—**.  
Claim 3, line 8, change "the predetermined" to **—a predetermined—**.  
Claim 3, line 9, before "first" insert **—different—**.  
Claim 3, line 15, before "first" insert **—different—**.  
Claim 4, line 1, change "A" to **—The—**.  
Claim 4, line 4, before "first" insert **—different—**.  
Claim 5, line 1, change "A" to **—The—**.  
Claim 5, line 7, before "linear" insert **—predetermined—**.  
Claim 6, line 1, change "A" to **—The—**.  
Claim 6, line 1, change "claim 3" to **—claim 5—**.  
Claim 6, line 3, before "data" delete **—the—**.  
Claim 6, line 4, change "the m-th dimension" to **—an m-dimensional—**.

- Claim 6, line 16, before "matrix" delete ~~the~~.
- Claim 6, line 22, delete ~~in said first step~~.
- Claim 7, line 1, change "A" to ~~The~~.
- Claim 7, line 5, change "m-th dimension" to ~~m-dimensional~~.
- Claim 8, line 1, change "A" to ~~The~~.
- Claim 9, line 7, before "first" insert ~~different~~.
- Claim 9, line 10, before "first" insert ~~different~~.
- Claim 9, line 15, before "first" insert ~~different~~.
- Claim 10, line 8, before "first" insert ~~different~~.
- Claim 10, line 11, before "first" insert ~~different~~.
- Claim 10, line 16, before "first" insert ~~different~~.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 1, 2, 9 and 10 are rejected under 35 U.S.C. 102(b) as being unpatentable over U.S. Patent No. 4,967,340 to Dawes.

6. As to Claim 1, Dawes shows and teaches the following subject matter:

- A method in design of a processing circuit for performing linear (transformation) operation on predetermined data – [col. 3, line 51 – 54]; Linear data processing operations (i.e., linear transform processings), , which is a **matrix multiplication**, typically involves "multiplying-and-accumulate (i.e., addition)" type of expressions ... processing (circuit) elements – multiplication element (multiplier) and addition element (adder) – [col. 3, lines 51 – 61]; linear transformation ... vector inner product ... matrix multiplication – [col. 1, lines 48 – 52]; Notice that (1) a linear transform processing involves

vector inner product (i.e., a first processing) and addition processing (i.e., a second processings) (2) each linear transform processing requires a different number of addition processings, which is dependent upon on the nature (e.g., rank) of the matrix, to be included in the (vector) inner product processing (3) due to hardwired configuration, required number of addition processings (second processings) to be included in the (vector) inner product processing of a linear transform processing should be identified/defined before designing the first processing (linear transform processing) – [col. 4, lines 21 – 38]; It is inherent that, to save design effort and share common device resources, addition processings performing the same number of additions on the same data in pluralities of linear transformation processings should be identified;

- Parallel signal processing techniques ... adaptive signal/data processing operation – [col. 1, lines 11 – 14]; **processing modules – modularity of (data) processing elements/cells** to facilitate **economic implementation** of data processing in parallel fashion and to achieve **high computational throughput** – [col. 1, lines 28 – 38]; Notice that, due to the modularity of (data) processing modules, inner product processing module for use in performing linear transformation is adaptively being shared and utilized by different first processing circuits and performing the identified number of addition processings, which is common to the different first processing circuits;
- Signal/data processing involves repetitive calculation (e.g., linear transform processing) – [col. 1, line 17 – 20].

It is inherent that, in order to efficiently and adaptively utilize the processing modules (1) common processing operations, which can be performed by the same set of processing modules, in different processing circuits in the processing circuit design should be identified (2) processing operations, which are not common to the processing circuits in the processing circuit design should also be identified and be treated separately.

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For reference purposes, the explanations given above in response to Claim 1 are called [Response A] hereinafter.

7. As to Claims 9 and 10, reasons are the same as recited in [Response A] given above.

8. As to Claim 2, reasons are included in [Response A] given above.

### ***Allowable Subject Matter***

9. Claim 3 – 8 are objected to as being dependent upon a rejected base claim, but they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Those claims are allowed is because that the prior art does not teach or fairly suggest the following subject matter:

- A circuit design method comprises a (third) step of defining a second linear transform by combining a number of first linear transforms corresponding to a predetermined number of times of processing for each of a plurality of different first processings in combination with other limitations as recited in Claim 3.

### ***Conclusion***

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun James Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272 - 1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin

Patent Examiner

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September 6, 2005

A handwritten signature in black ink, appearing to read "James Lin", is written over the printed name and date.